IN THE CLAIMS

1. (Currently Amended) An integrated circuit comprising a built-in self test (BIST) state machine, having:

a plurality of states to conduct a plurality of tests for a random access memory (RAM), each state capable of performing a null operation, a write operation, a read operation, and a read/write operation;

a command register coupled to the plurality of states ~~and storing a~~to store test ~~pattern~~ data for use with the plurality of states; and

an address counter coupled to the plurality of states to determine a test location in the RAM.

2. (Currently Amended) The integrated circuit of claim 1, wherein the plurality of states consists of only four states to ensure that no more than four state~~s machines~~ are used by the BIST state machine for a test.

3. (Original) The integrated circuit of claim 1, wherein one of the plurality of states is an idle state to which the BIST state machine returns after a final address or an error is detected.

4. (Original) The integrated circuit of claim 1, wherein one state of the plurality of states assigned to perform the null operation is skipped during transitioning between the plurality of states.

5. (Original) The integrated circuit of claim 1, further comprising an additional counter to cause a state to repeat an assigned operation.

6. (Original) The integrated circuit of claim 1, wherein the address counter is incremented whenever a first state transitions to itself in a single state chain or to a second state positioned prior to the first state in a multiple state chain.

7. (Original) A method, comprising:

feeding a test pattern to a command register in a built-in self testing (BIST) state machine;

reading a test location in a random access memory (RAM) from an address counter; and

applying the commands of the test pattern to the test location using a plurality of states, each of the plurality of states being configurable to perform a null operation, a write operation, a read operation, and a read/write operation.

8. (Currently Amended) The method of claim 7, wherein the plurality of states consists of only four states to ensure that no more than four state<u>s</u> ~~machines~~ are used by the BIST state machine.

9. (Original) The method of claim 7, further comprising returning to an idle state after an error is detected or to which the BIST state machine returns after a final address is read.

10. (Original) The method of claim 7, further comprising repeating an assigned operation based on contents of a counter.

11. (Original) The method of claim 7, further comprising skipping a state assigned to perform a null operation.

12. (Original) The method of claim 7, further comprising incrementing an address counter whenever a first state transitions to itself in a single state chain or to a second state positioned prior to the first state in a multiple state chain.

13. (Original) The method of claim 7, further comprising signaling an address counter to increment or decrement addresses when advancing.

14. (Original) The method of claim 7, further comprising signaling to the BIST state machine to read from both a static address and the test location.

15. (Original) The method of claim 7, further comprising inverting data based on a least significant address bit.

16. (Original) A machine-readable storage medium tangibly embodying a sequence of instructions executable by the machine to perform a method comprising:

feeding a test pattern to a command register in a built-in self testing (BIST) state machine;

reading a test location in a random access memory (RAM) from an address counter; and

applying the commands of the test pattern to the test location using a plurality of states, each of the plurality of states being configurable to perform a null operation, a write operation, a read operation, and a read/write operation.

17. (Currently Amended) The machine-readable storage medium of claim 16, wherein the plurality of states consists of only four states to ensure that no more than four state~~s~~ ~~machines~~ are used by the BIST state machine for a test.

18. (Original) The machine-readable storage medium of claim 16, further comprising returning to an idle state after an error is detected or to which the BIST state machine returns after a final address is read.

19. (Original) The machine-readable storage medium of claim 16, further comprising repeating an assigned operation based on contents of a counter.

20. (Original) The machine-readable storage medium of claim 16, further comprising skipping a state assigned to perform a null operation.